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A Celestica Company

Designing SOSA™ Backplanes for the Future of Electronics

DESIGN › DEVELOP › DEPLOY

50 Years
1972-2022

Designing SOSA™ Backplanes for the Future of Defense Electronics

The Cold War is a topic for history lessons, no longer a useful paradigm for defining defense programs. We now face a global adversary that is technically agile and future-focused. If our programs cannot respond at a competitive pace, our warfighters will lose the powerful technology advantage they've wielded for over 75 years.

Key to maintaining that advantage is the ability to rapidly insert new, more powerful technology into deployed sensor-enabled systems for radar, EO/IR, SIGINT, EW, and Communications. That is the most critical issue driving a change in defense electronics procurement, but not the only issue. The economics of new program development and deployment is also a concern, with an increasing focus on full lifecycle costs The Sensor Open Systems Architecture™ (SOSA™) is a comprehensive standard developed to address these issues and driven by the Department of Defense (DoD), with industry support. SOSA includes both Business Architecture and Technical Architecture. This paper will focus on a specific technical topic, signal integrity, leaving the discussion of planning and acquisition topics to other forums.

Backplane signal integrity is an emerging issue for new SOSA systems. The issue isn't caused by the standard; it arises because new systems must be able to operate at very high data signaling rates to keep pace with exploding volumes of sensor-generated data. There are design techniques to mitigate the effects of signal integrity issues but effective application of those techniques demands analysis, modeling, and testing.

Longstanding Program Issues Are Becoming Critical

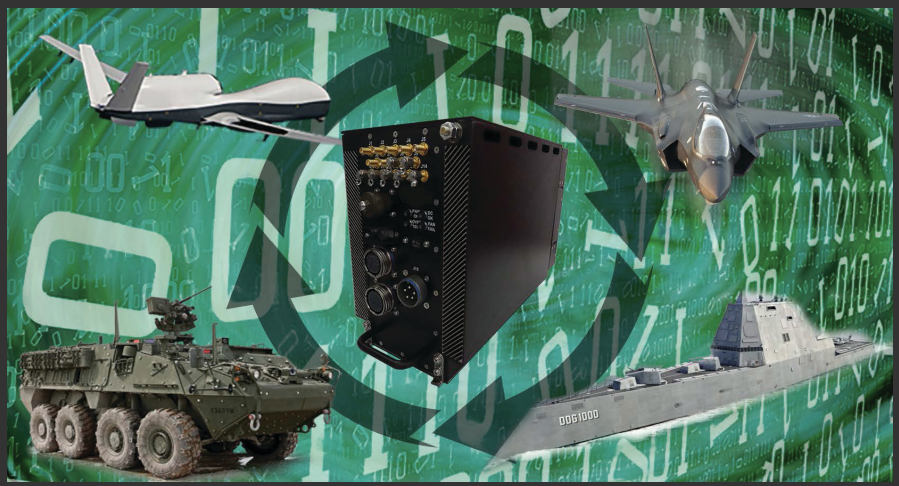
The DoD has long struggled with lengthy technology upgrade cycles that usually involve the replacement of complete systems. These complex 'forklift upgrades', including not just a system chassis but also new power and communications cabling, delay the deployment of embedded technology. The result is that deployed processors, A/D converters, and memory chips all fall behind state-of-theart commercial components, often by several generations.

In addition, most of the electronic modules deployed ontoday's defense platforms are built to current standards but are not really interoperable. Interoperability, a stated goal in many programs, has almost never been achieved in any practical sense. Vendor lock-in is common because small customizations in hardware and unique supporting software make switching vendors an expensive effort involving hundreds of systems changes.

In fairness, there are benefits to vendor lock-in. Going allin with a single vendor can allow programs to simplify functions like interfaces and become, in the short-run, more agile. It can also potentially achieve better quality, as single-vendor solutions are often very tightly integrated.Despite that, vendor lock-in and the absence of true interoperability drive-up system lifecycle costs and contribute to the pattern of lengthy technology upgrades.

While these issues have made ongoing program development more difficult, historically they have not seriously impacted our warfighting capabilities. However, as mentioned earlier, we now face an adversary that is rapidly advancing its own defense technologies, while stealing ours whenever possible. Staying ahead is a challenge; falling behind is unthinkable. In parallel, embedded designs and deployments are being stressed by exploding sensor volumes. Mission-critical defense systems already employ seemingly countless sensors, with numbers that keep increasing. They feed applications that continually demand expanded capability from each sensor- more detailed images, the ability to track more targets, and a comprehensive view of the electromagnetic spectrum. The result is a geometric increase in sensor data volumes, forcing systems to implement continual leaps in internal operating bandwidth.

For both adversarial and sensor technology reasons, we simply must resolve our issues with lifecycle costs, interoperability, and, most importantly, the speed of deployed technology upgrades. That brings us to SOSA.



The goals of the SOSA standard are to:

- Enable upgrades of system elements without redesigns
- Drive more competitive, cost-effective acquisitions
- Lower system lifecycle costs
- Encourage commonality and reuse of components
- Enable interoperability between systems

Summarizing SOSA

SOSA standard development and definition is managed by the SOSA Consortium, consisting of the Air Force, Navy, Army, other government agencies, and industry. SOSA, aligned with MOSA, brings together elements of standards from all three services. SOSA is leveraging other already existing standards efforts. Starting at a high level, it is aligned with the DoD's Modular Open Systems Approach (MOSA) in a focus on using standardized hardware and software. SOSA also brings together elements from standards developed by each of the three military services, specifically:

- The Army's CMOSS (C4ISR Modular Open Suite of Standards), MORA (Modular Open Radio Frequency Architecture), and VICTORY(Vehicular Integration for C4ISR/EW Interoperability)
- The Navy's HOST (Hardware Open Systems Technology),
- The Air Force's SOA (Service Oriented Architecture) and UCI (Universal Command and Control Interface).

At a technical level, SOSA adopted concepts and definitions from the OpenVPX standard, including a taxonomy of Planes, Pipes, and Profiles. However, SOSA accepted only a small subset of the OpenVPX profile options. OpenVPX has quite a few Plug-In Card( ) Profiles (PICPs) that are largely redundant. To simplify that situation, while allowing flexibility, SOSA uses the concept of a pinout 'overlay' to define the functionality of previously undefined pins.

SOSA also reduces the number of protocol implementations defined within OpenVPX, though the new standard does maintain flexibility by expanding on the OpenVPX Alternate Profile Module Scheme with specific fields for RF pinouts, XMC overlay, and Switch Front Panel Fiber I/O.

The result is that actual SOSA systems will look like OpenVPX systems but with a huge reduction in variability. A much more tightly defined technical specification means that cards will be interoperable between systems, and backplanes will be pin-compatible with a wide range of cards from a variety of vendors.

High-bandwidth SOSA Backplanes and Signal Integrity

While component interoperability will be greatly simplified, real-world SOSA systems face a significant challenge in supporting the demands of incredibly high bandwidth sensor systems. At a practical level, this means implementing new generations of interconnects, specifically PCIe Gen4 and 100 GbE. System designers are now discussing requirements in terms of 'Gen-4/5 bandwidths', where Gen-4 means PCIe Gen4 and Gen-5 is shorthand for 100 GbE( ).

It is worth noting that SOSA has a prominent place for the Ethernet protocol. Within the interconnects definitions it is specified for use in both the general purpose Message Interconnect and the higher data rate Wideband Low-Latency Interconnect.

Card vendors (sensor interfaces, processors, etc.) are already bringing to market products that support these new generations of high-speed interconnects, a requirement for keeping up with the bandwidth explosion in sensor systems. SOSA aligned versions of these cards will certainly appear soon and, in some cases, they have already been announced.

However, configuring these cards into powerful SOSA aligned systems requires backplanes that also support those high bandwidth Gen-4/5 interconnects for communications between cards. That introduces a complex technical issue, signal integrity.

Usually measured in terms of Bit Error Rate, signal integrity refers to the quality of an electrical signal. All signals are affected, to some degree, by noise, distortion, and loss. Each of these integrity issues can be caused by a variety of factors, including signaling speed (bit rate), distance traveled by the signal, transmission material, surrounding materials, and proximity to other signals.

Digital systems can deal with small disruptions in signal integrity through the Error Checking and Correction process common to communications protocols. However, if the number of disruptions increases, data rates plummet as more and more communications packets must be resent. At some point, a high number of disruptions will make system operations impossible.

Most circuits can operate with acceptable signal integrity over short distances and at low bit rates. Things become more problematic as travel distances and signal speeds increase. In a complex system, with hundreds of high-speed signals carried by wire traces laid out in a small space, unmitigated signal integrity issues will make operations unreliable and unacceptable.

Signal Integrity at Gen-4/5 Signaling Rates

As discussed earlier, SOSA backplanes are defined with the same concepts and topology as OpenVPX backplanes, just fewer options. They look the same and operate in the same fashion, which makes for a good deal of continuity as system designers move forward from OpenVPX to SOSA.

The big change with the new SOSA backplanes is not directly related to the SOSA standard but in the support for a leap slot-to-slot signaling rate. The current generation of OpenVPX systems usually referred to as Gen-3, use 8 to 10 Gbaud signaling rates. The VITA standards body has worked to define specifications for the Gen-4/5 data transfer speeds that can meet exploding sensor processing requirements. The SOSA standard definitions are benefitting from that work.

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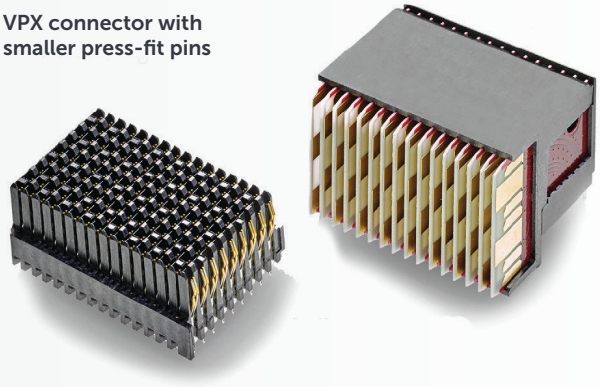
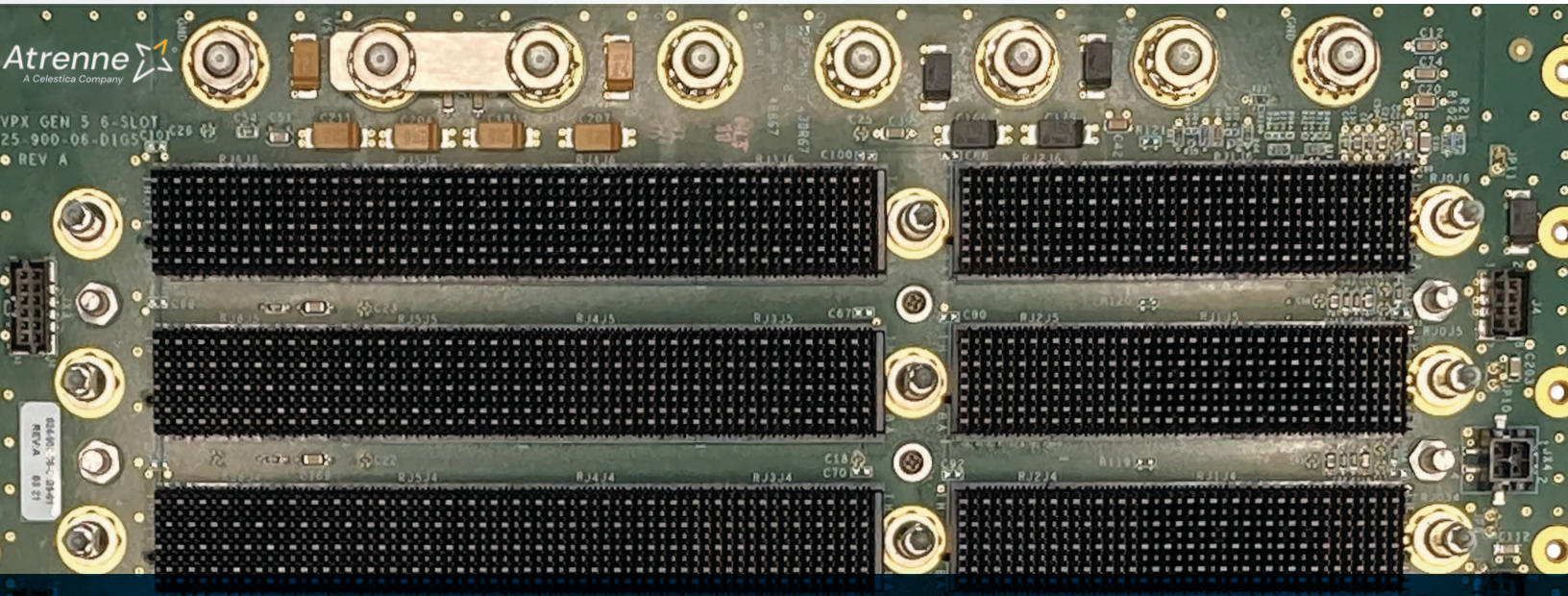
Gen-4/5 SOSA backplanes will need to support a daunting set of copper high-speed serial protocols, including PCIe Gen4 and 100 GbE. Early tests have shown an explosion of signal integrity issues at these higher data rates. It is clear that some of today's Gen-3 backplane designs may already have the pins to support the defined SOSA slot profiles but they cannot operate at new generation speeds.

These systems can be impacted by a wide range of signal integrity issues, including ringing, crosstalk, ground bounce, insertion loss, and power supply noise. However, for OpenVPX systems, crosstalk and insertion loss are usually the most significant signal integrity problems. It is safe to assume that will extend to SOSA systems.

VPX connector with smaller press-fit pins





One specific problem area is the legacy VPX connectors; they are no longer able to handle the higher signaling rates across a realistic range of modules and backplane trace lengths. Fortunately, improved versions of the VPX connector with smaller press-fit pins are now available, delivering improved signal integrity performance. These new connectors are fully compatible and interoperable with the original VPX connectors but provide reliable performance in the 25 Gbaud range.

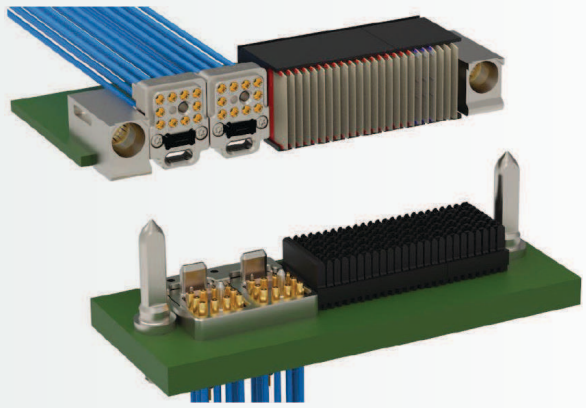
Unfortunately, connectors are just one piece of the signal integrity problem for Gen-4/5 SOSA systems. Long traces in a backplane can cause issues, as can temperature-induced changes, and manufacturing variations. Perhaps most significant are signal integrity issues introduced by system materials. For example, the fiberglass weave that is used in a backplane substrate often introduces wave skew into signals carried by differential pairs, an effect that increase substantially at higher signaling rates **(see sidebar A Complex Signal Integrity Problem - Fiber Weave Skew).**

Design issues are further complicated because signal integrity is a cumulative performance issue. All of the potential signal integrity problem areas must be considered early in the system design process. Certain modeling techniques can be used to gain insights and explore design alternatives. Then prototypes should be tested using a range of configurations to determine if signal integrity issues have been resolved or if additional modifications are required.

Bringing High-Performance SOSA Backplanes to the Defense Community

Atrenne's expertise is centered on providing innovatively designed electronics solutions that exceed performance criteria and do not fail in critical applications. For over 50 years, our design teams have developed hundreds of chassis enclosures and backplanes to meet the most rigorous defense systems requirements. They are deployed today across multiple programs in a variety of platforms, operating under a range of harsh environmental conditions.

Our experience in addressing signal integrity issues has developed across advancing generations of standards and geometric increases in signaling rates. We successfully developed backplane designs to support the transition from 6.25 Gbaud Gen-2 systems to >10Gbaud Gen-3 designs. Now we are building on what we learned in that transition to deliver SOSA backplanes that support Gen-4/5 data rates with reliable and consistent signal integrity.



Our design teams also follow a comprehensive set of backplane design rules that include:

- Trace length optimization
- Materials selection
- Weave skew mitigation
- Stack-up optimization
- Via tuning and crosstalk reduction
- Controls for manufacturing tolerance variations

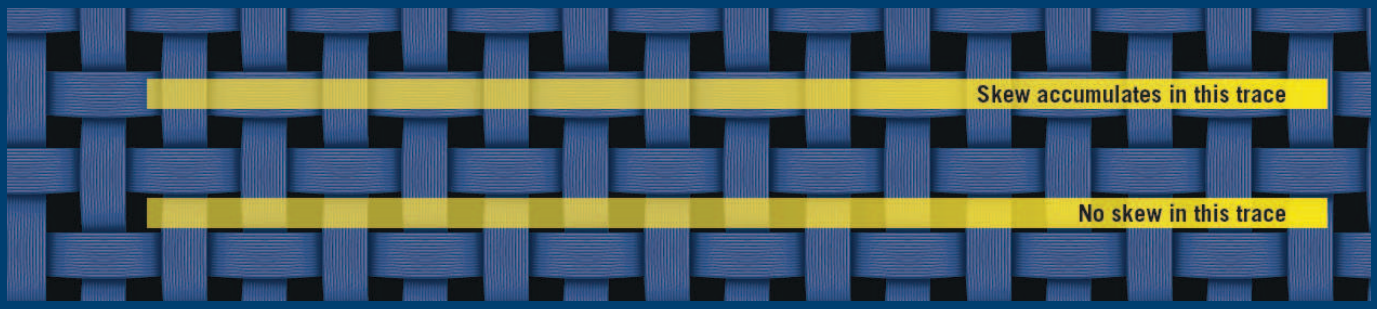
An important component of our SOSA backplane design process is using three-dimensional full-wave electromagnetic (EM) field modeling. As data signal interactions become increasingly complex at very high data rates, simplified modeling tools, which assume one dominant dimension, cannot be relied upon for accurate projections.

We recently announced a family of high-performance 3U, 6U, and hybrid 3U/6U backplanes designed to meet the demanding signal integrity requirements of PCIe Gen4 and 100GbE. You can read about the details of our signal integrity modeling, tests, and design rules in the Gen-4/5 OpenVPX Signal Integrity white paper.

Engage with Atrenne to Discuss a Next-Generation SOSA backplane for Your Program

With more than 50 years of experience, Atrenne harnesses the power of engineering innovation and integration to develop application-specific solutions that provide exceptional value to our customers. We've learned that all our innovations are complemented and enhanced by collaborating with our customers to solve problems. Engage with our team to explore how they can meet your most demanding backplane requirements and help move your new SOSA-based programs forward.

Sidebar



Skew arises when traces are routed over different portions of the fiber weave.

Longstanding Program Issues Are Becoming Critical

Fiber weave skew is not a signal integrity problem at lower signaling rates. At the system level, it was first recognized as a concern when backplanes were designed to support Gen3 10 Gbaud systems. Analysis and tests show that the effect will be magnified further with the move to even higherspeed SOSA systems.

The issue is rooted in the fiberglass weave used to form a backplane substrate. Fiberglass strands are woven together, then covered with resin to form a specified section. After the resin hardens, the sections can be layered.

The dielectric constants of these two materials, fiberglass, and resin are very different. This difference is exacerbated by cavities that form in the resin as it hardens. As a signal traverses a trace and the electromagnetic field passes through the substrate material, the dielectric constant seen by the signal varies along the length of the interconnect. The cavities also cause the velocity of a signal to vary as it passes through the substrate. The overall effect is a skew between two ends of a differential pair. When one trace in a pair passes over a cavity, or just significantly more resin than fiber, the skew builds. The higher the signaling rate, the more pronounced the skew. Over the length of a backplane interconnect the skew will accumulate and eventually the two trace signals will no longer be synchronized and signal integrity will be lost.

Design approaches to mitigate these issues include a tighter weave for the fiberglass, special resins, and routing signals at an angle to the fiberglass weave. These approaches can, of course, be used in combination.

This is an exciting capability, with almost limitless options for innovative mechanical designs. Our engineering team is currently exploring some of these options and would value the opportunity to collaborate with your team on new ideas and customized implementations.

Atrenne®
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General Inquires: +1 800 926 8722

Atrenne Computing Solutions Division, US: +1 508 588 6110

sales@atrenne.com | atrenne.com

in Atrenne | @AtrenneOfficial | f @AtrenneIntegratedSolutions