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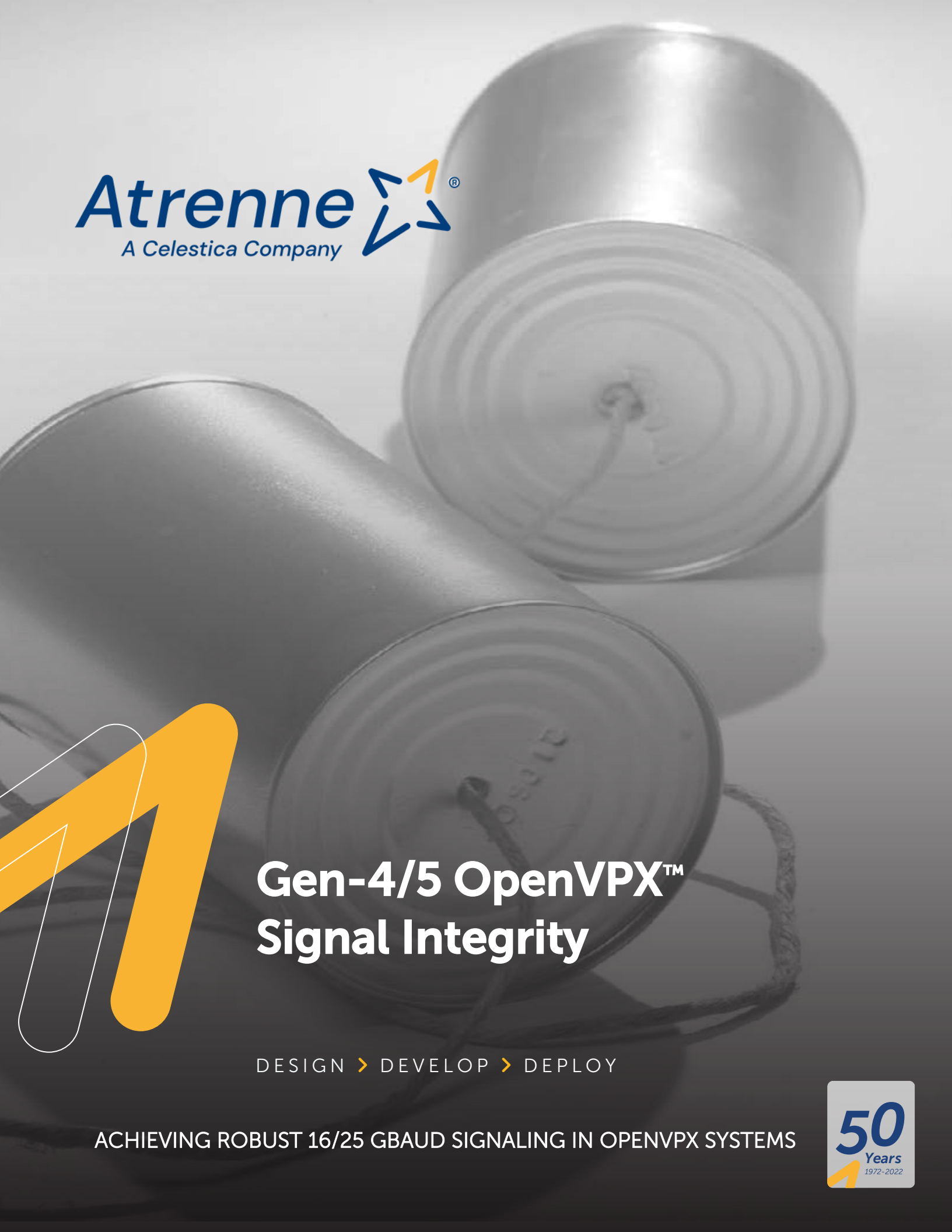


Gen-4/5 OpenVPX™ Signal Integrity

DESIGN › DEVELOP › DEPLOY

ACHIEVING ROBUST 16/25 GBAUD SIGNALING IN OPENVPX SYSTEMS

50 Years 1972-2022

Gen-4/5 OpenVPX™ Signal Integrity

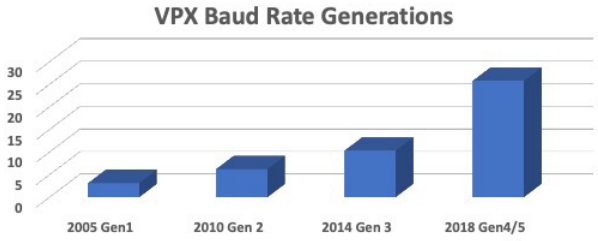
Achieving robust 16/25 gbaud signaling in OpenVPX systems

The challenge: Robust operation of 100 Gb Ethernet and PCI Express Gen-4 on your processing system, even in the most challenging environmental conditions. These high-speed serial fabrics utilize 16/25 Gbaud signaling. Until recently, this was not possible in an OpenVPX system. Using a new generation of connectors along with highly-optimized backplane and module designs, OpenVPX applications can now confidently run 16 Gbaud Gen-4 and 25 Gbaud Gen-5 interconnects, raising system performance to a whole new level. In this white paper, we discuss some of the difficulties that were overcome to achieve this much higher level of throughput.

MOVING UP FROM 8/10.3 Gbaud TO 16/25 Gbaud IS A WHOLE NEW BALL GAME

While Signal Integrity (SI) has been an important consideration for OpenVPX systems designers from its very inception, the critical challenges that SI posed for obtaining optimal performance first became a significant issue over the last five years as the industry transitioned from Gen-2 to Gen-3 signaling at 8/10 Gbaud. While making this transition, many suppliers encountered SI issues at Gen-3 signaling rates that required greater levels of engineering expertise than had been required with Gen-2. But this was just a warm-up for today's challenges with the next step-up in baud rates.

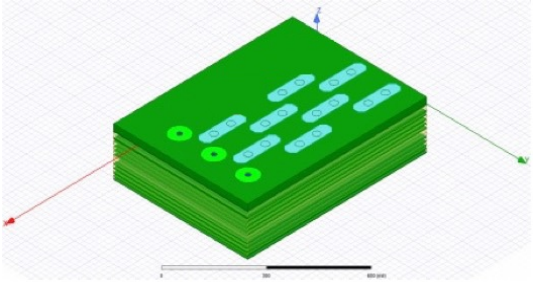
Today, the OpenVPX™ (VITA 65.x) ecosystem is transitioning from Gen-3 to Gen-4/Gen-5 signaling, which drives and increase in signaling rates from 8/10 Gbaud to >25 Gbaud. Increasing the bandwidth by more than 2.5-times causes significant design challenges, starting with the VPX connector system.



3D FULL-WAVE EM FIELD MODELING IS NOT OPTIONAL FOR 16/25 Gbaud

When making the move to Gen-4/Gen5 signaling, it is important to understand that this transition will require another significant increase in the level of SI tools, capability, expertise, and know-how to ensure successful design and implementation of your OpenVPX system.

Many designers are accustomed to using quick short-cut field solvers, which were actually marginal at 8/10 Gbaud rates. At 16/25 Gbaud rates, anything less than a top-quality full wave field solver is no longer an option. A 2.5D field solver will give inaccurate results and it is just not good enough anymore!



IMPROVED VPX CONNECTORS HELP

The VPX connector system was originally designed for 6.25 Gbaud signaling rates. With the new >25 Gbaud Gen-5 OpenVPX signaling rates, the existing

VPX connector was no longer able to handle the higher signaling rates with a realistic range of module and backplane trace lengths.

Improved versions of the VPX connector with smaller press-fit pins are now available, providing better signal integrity performance (ANSI/VITA 46.30). These new connectors are fully compatible and interoperable with the original VPX connectors, but they support improved signal integrity which is needed at >25 Gbaud Gen-5 OpenVPX signaling rates.

BUT IMPROVED CONNECTORS ARE NOT ENOUGH

As you prepare to design OpenVPX systems with the new Gen-4/Gen-5 signaling rates, it is important to understand the higher level of skill required and the important role that SI plays with the new faster bandwidth rates. The risk is that Gen-4/Gen-5 SI issues can and will wreak havoc on your program if you are not prepared to address and mitigate them.

Some of the key Signal Integrity issues that have become table stakes for Gen-4/5 include:

- Full 3D electromagnetic field modeling of vias and traces – we use HFSS™, the most trusted field solver in the industry. Lesser solvers that use shortcuts to run faster will not provide accurate simulation results.
- Accurate modeling of all losses is required, including dielectric loss, skin effect loss, surface roughness loss.
- Manufacturing variation and temperature variation of losses need to be taken into account because they have a huge effect on Gen4/5 results
- The ultra-low skew designs that are needed for Gen4/5 require mitigation of fiber weave skew at a whole new level for VPX.

GETTING READY FOR 16/25 GBAUD SIGNALING

In anticipation of this technology transition, Atrenne Computing Solutions has been studying >10 Gbaud signaling for several years (see our earlier White Papers

- 10 Gbaud signaling with VPX (2010)
- The importance of signal integrity: achieving robust GEN-3 >10 GBAUD signaling in OpenVPX systems (2013)

As the VPX connector approaches its performance limits. Atrenne Computing Solutions has done extensive research, including with partners, to develop best practices for attaining reliable and robust signal integrity performance with Gen-4/Gen-5 OpenVPX systems.

We have developed comprehensive and advanced internal SI analysis capabilities and resources. For Gen-4/5, we performed extensive signal integrity studies in order to:

- Develop measured fiber weave skew data that we can trust. There are a lot of conflicting measurement-based papers on this topic, so we needed to sort this out.
- Leverage our patented VPX signal integrity optimizations with the improved VPX connectors, optimizing design of VPX connector vias for signal integrity, improving insertion loss, return loss and crosstalk.
- Leverage simulation and measurement correlation for 16/25 Gbaud rates.

FIBER WEAVE SKEW FOR 16/25 GBAUD IS A REALLY BIG PROBLEM – YIKES!

At 25 Gbaud, the Unit Interval (UI) is less than 38 pico seconds (ps), so the total end-end skew for a backplane plus two modules must be much less than this amount of skew. With fiber weave skew predictions of 1 ps/inch or more, we knew that this was a major issue for Gen-4/5.

There are a lot of measurement-based papers on fiber weave skew effect that provide a jumble of conflicting skew predictions that tend to be overly optimistic; that's because there was a flaw in the way that most of these measurements were done.

With a better approach we were able to cut through that misinformation with measured fiber weave skew data that we can trust, and we have used this data to develop design rules to achieve the ultra-low skew designs that are needed for 16/25 Gbaud operation.

GETTING THE MOST OUT OF THE IMPROVED VPX CONNECTOR

Although the ANSI/VITA 46.30 improved VPX connectors support 16/25 Gbaud operation, we wanted to support longer backplanes at these higher speeds.

Leveraging our patented Signal Integrity technology utilized in our Gen3 backplanes, we utilized 3D EM field modeling in HFSS to develop some additional Signal Integrity technology that improves return loss, ISI, and crosstalk in the backplane design.

16/25 GBAUD SI MODELING and TEST RESULTS

The results of the SI modeling have provided us with very useful data that helps define best- practice rules for designing OpenVPX systems with Gen 4/5 signaling rates. To mitigate the SI impairment issues associated with the VPX connector requires the optimization of several design parameters:

- Backplane trace length optimization
- Backplane materials selection
- Backplane weave skew mitigation
- Backplane stack-up optimization
- Backplane via tuning and crosstalk reduction
- Controlling backplane manufacturing tolerance variations
- Accounting for worst-case manufacturing variation, temperature variation, and skew variation

Atrenne Computing Solutions has developed a complete set of design rules to ensure a robust 16/25 Gbaud backplane design.

We have also performed complete end-to-end modeling over various backplane lengths to ensure robust performance at the system level.

END-END PCIe Gen 4 COMPLIANCE AT 16 GBAUD USING SEASIM

PCIe Gen4 performance can be validated utilizing the SEASIM tool that was developed by PCI-SIG.

SEASIM is an open-source simulation tool that provides turnkey capability for channel assessment, where the user provides the channel characteristics using one or more touchstone (s-parameter) files, and the tool calculates a statistical eye showing eye height and width that can be compared to PCIe pass/fail limits.

Unlike lower speed protocols, the channel includes the device packages at both ends. The PCIe Specification defines worst-case device package characteristics that can be added to the channel if an actual device package model is not available. See Figure 1. for the end-end PCIe channel configuration that we simulated.

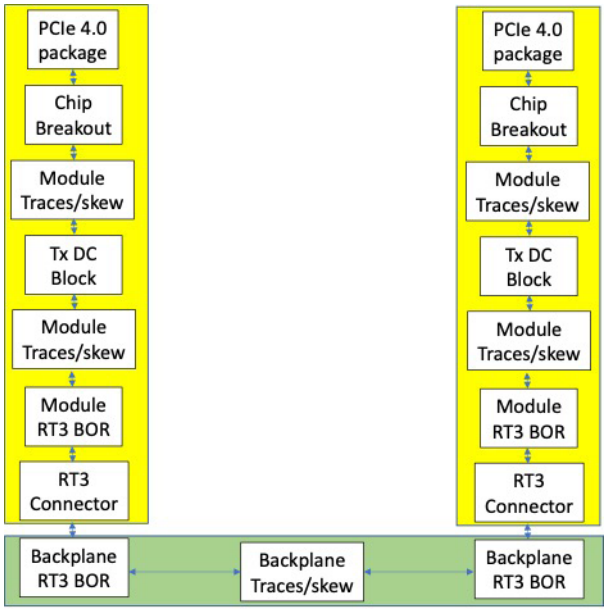


Figure 1. Channel Topology for PCIe Gen4 Seasim Simulations

Per the PCIe 4.0 specification, the PCIe pass/fail limits are +/-15 mV eye height and 0.3 UI Eye Width. We used Seasim revision 1.06 for our analysis.

Here are Long-Long channel Seasim Eye Diagram plots with Modules at both ends using 6-inch long 5-mil VPX Module traces using Megtron 6 as well as generic VPX Module BOR (break out region) via configurations per TE Connectivity's suggested breakout and via geometries but with longer (6-inch) Module traces. The module channels each include 5 ps worst-case skew and standard PCIe Gen4 NRC reference packages.

The backplane in this case is Atrenne's long 14" trace length high-performance backplane including 5 ps worst-case skew.

These results are for even wafer BC victim Rx pair and odd wafer AB victim Rx pair with mismatched Low-High-Low impedances and maximum 15 ps total channel skew. This represents the worst-case configuration using Atrenne's backplane design rules.

As can be seen from the plots, the BC victim pair channel passes with 34.82 mV Eye Height and 0.362 UI Eye Width, and the AB victim pair channel passes with 38.42 mV Eye Height and 0.386 UI Eye Width.

Note that actual device package performance is expected to perform better than the worst-case PCIe Gen4 NRC reference package, which would yield even better Eye Diagram results.

Atrenne Computing Solutions has developed a complete set of design rules to ensure a robust 16/25 Gbaud backplane design.

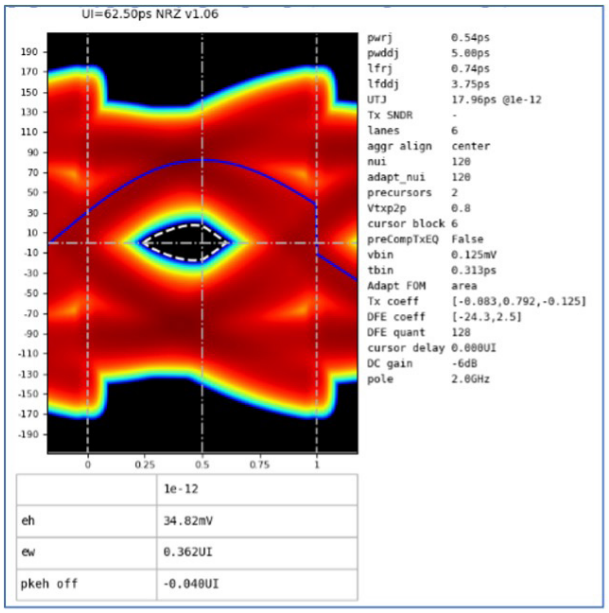


Figure 2. Atrenne Long Channel BC Victim Pair Eye Diagram

Here are Short-Short channel Seasim Eye Diagram plots with Modules at both ends using 4-inch long 5-mil VPX Module traces using Megtron 6 as well as generic VPX Module BOR (break out region) via configurations per TE Connectivity's suggested breakout and via geometries but with shorter (4-inch) Module traces. The module channels each include 5 ps worst-case skew and standard PCIe Gen4 NRC reference packages.

The backplane in this case is Atrenne's 1.5-inch minimum trace length high-performance backplane including 5 ps worst-case skew.

These results are for even wafer BC victim Rx pair

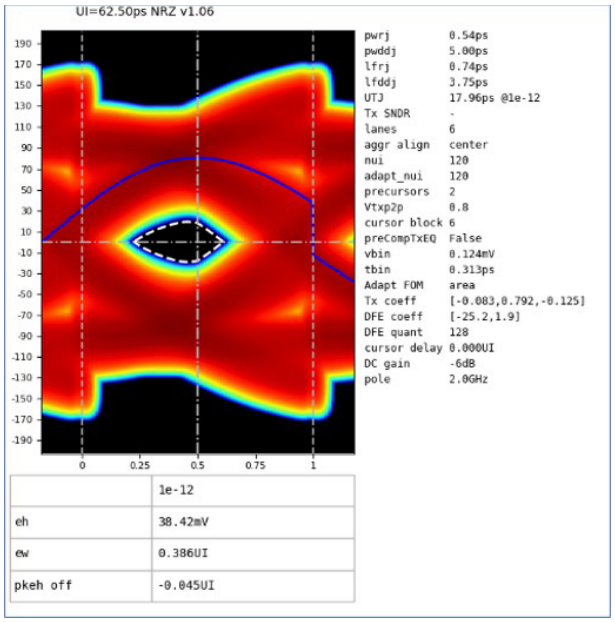


Figure 3. Atrenne Long Channel AB Victim Pair Eye Diagram

and odd wafer AB victim Rx pair with mismatched Low-High-Low impedances and maximum 15 ps total channel skew. This represents the worst-case configuration using Atrenne's backplane design rules. As can be seen from the plots, the BC victim pair channel passes with 83.47 mV Eye Height and 0.314 UI Eye Width, and the AB victim pair channel passes with 84.27 mV Eye Height and 0.325 UI Eye Width. Note that actual device package performance is expected to perform better than the worst-case PCIe Gen4 NRC reference package, which would yield even better Eye Diagram results.

Here are Long-Long channel Seasim eye diagram plots

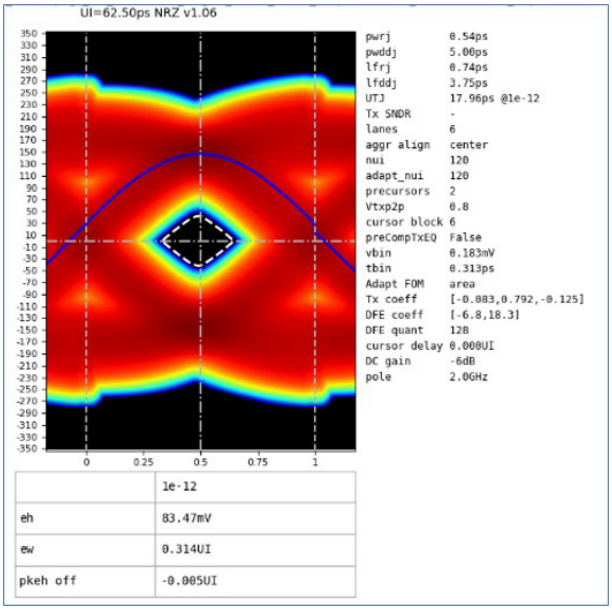


Figure 4. Atrenne Short Channel BC Victim Pair Eye Diagram

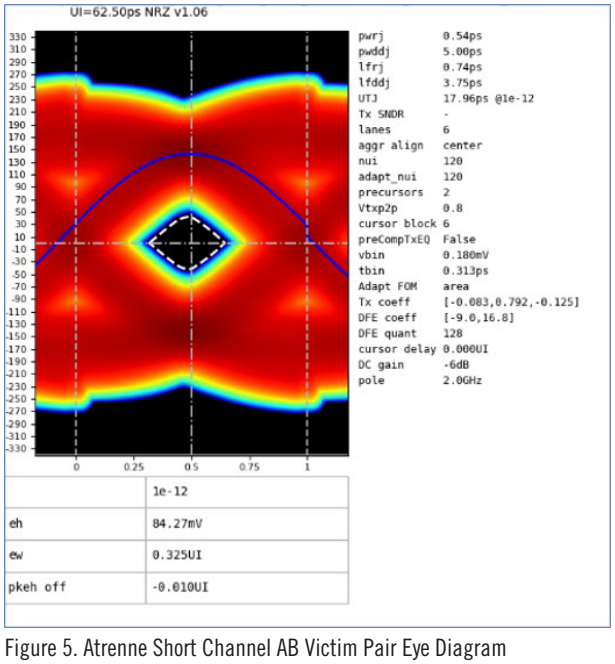


Figure 5. Atrenne Short Channel AB Victim Pair Eye Diagram

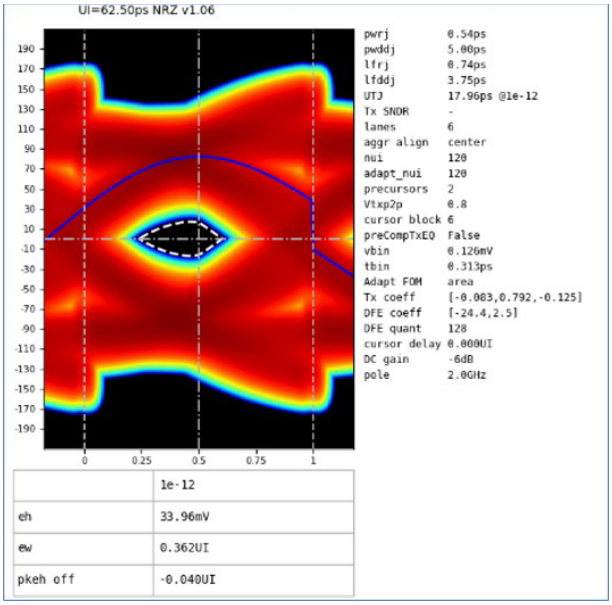


Figure 6. TE-spec Long Channel BC Victim Pair Eye Diagram

with Modules at both ends using 6-inch long 5-mil VPX Module traces using Megtron 6 as well as generic VPX Module BOR (break out region) via configurations per TE Connectivity's suggested breakout and via geometries but with longer (6-inch) Module traces. The module channels each include 5 ps worst-case skew and standard PCIe Gen4 NRC reference packages.

The backplane in this case is a backplane using generic BOR (break out region) via configurations per TE Connectivity's suggested breakout and via geometries as well as the same trace length as Atrenne's long 14" trace length high-performance backplane including 5 ps worst-case skew.

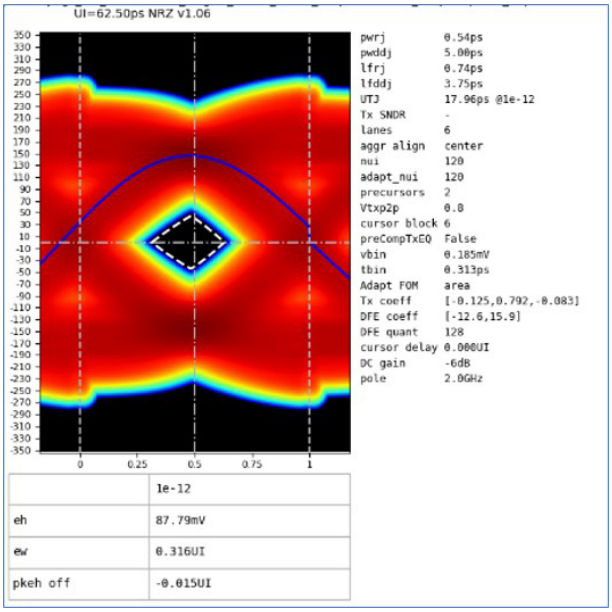


Figure 8. TE-spec Short Channel BC Victim Pair Eye Diagram

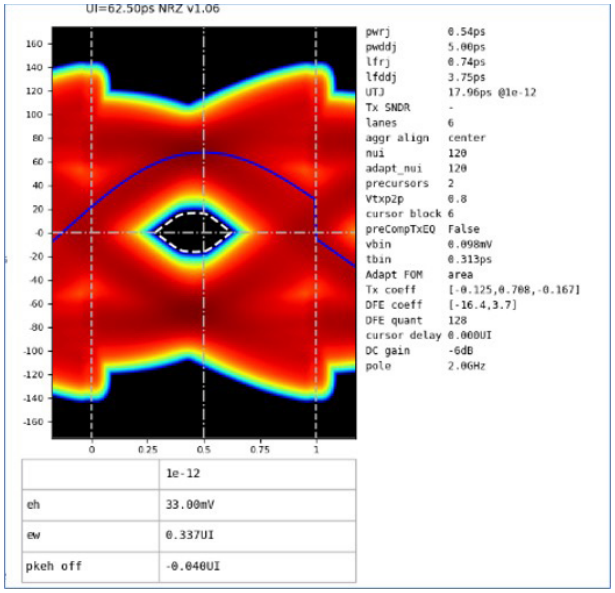


Figure 7. TE-spec Long Channel AB Victim Pair Eye Diagram

These results are for even wafer BC victim Rx pair and odd wafer AB victim Rx pair with mismatched Low-High-Low impedances and maximum 15 ps total channel skew. This represents the worst-case configuration using Atrenne's backplane design rules.

As can be seen from the plots, the BC victim pair channel passes with 33.96 mV Eye Height and 0.362 UI Eye Width, and the AB victim pair channel passes with 33.0 mV Eye Height and 0.337 UI Eye Width. Note that actual device package performance is expected to perform better than the worst-case PCIe Gen4 NRC reference package, which would yield even better Eye Diagram results.

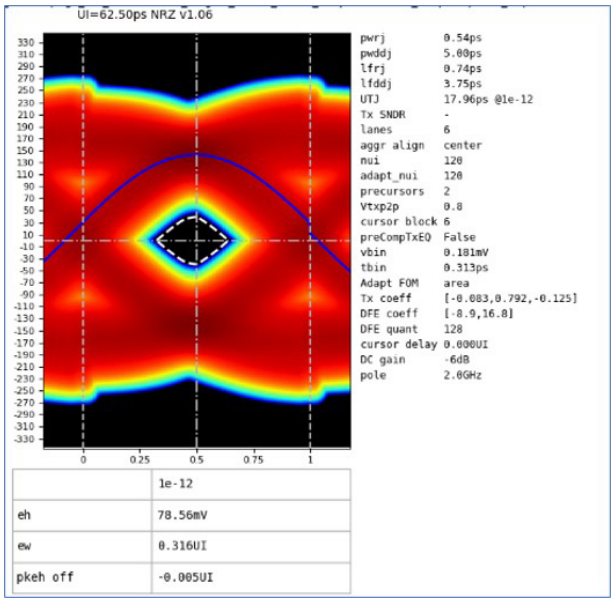


Figure 9. TE-spec Short Channel AB Victim Pair Eye Diagram

Here are Short-Short channel Seasim Eye Diagram plots with Modules at both ends using 4-inch long 5-mil VPX Module traces using Megtron 6 as well as generic VPX Module BOR (break out region) via configurations per TE Connectivity's suggested breakout and via geometries but with shorter (4-inch) Module traces. The module channels each include 5 ps worst-case skew and standard PCIe Gen4 NRC reference packages.

The backplane in this case is a backplane using generic BOR (break out region) via configurations per TE Connectivity's suggested breakout and via geometries as well as the same 1.5-inch trace length as Atrenne's minimum trace length high-performance backplane including 5 ps worst-case skew.

These results are for even wafer BC victim Rx pair and odd wafer AB victim Rx pair with mismatched Low-High-Low impedances and maximum 15 ps total channel skew. This represents the worst-case configuration using Atrenne's backplane design rules.

As can be seen from the plots, the BC victim pair channel passes with 87.79 mV Eye Height and 0.316 UI Eye Width, and the AB victim pair channel passes with 78.56 mV Eye Height and 0.316 UI Eye Width. Note that actual device package performance is expected to perform better than the worst-case PCIe Gen4 NRC reference package, which would yield even better Eye Diagram results.

Both the short channel and the long channel pass Eye Height and Eye Width requirements for PCIe Gen4 with lots of margin for both the TE spec backplane and the Atrenne backplane, although Atrenne's backplane performs slightly better.

Case	Module	Back-plane	Conn	Eye Diagram	Compare Results
Long BC pair	TE spec	Atrenne	RT3	EH: 34.82 mV EW: 0.362 UI	Worst-case Atrenne EH 1.82 mV better / EW 0.025 UI better
	TE spec	TE spec	RT3	EH: 33.96 mV EW: 0.362 UI	
Long AB pair	TE spec	Atrenne	RT3	EH: 38.42 mV EW: 0.386 UI	
	TE spec	TE spec	RT3	EH: 33.0 mV EW: 0.337 UI	
Short BC pair	TE spec	Atrenne	RT3	EH: 83.47 mV EW: 0.314 UI	Worst-case Atrenne EH 4.91 mV / EW 0.002 UI worse
	TE spec	TE spec	RT3	EH: 87.79 mV EW: 0.316 UI	
Short AB pair	TE spec	Atrenne	RT3	EH: 84.27 mV EW: 0.325 UI	
	TE spec	TE spec	RT3	EH: 78.56 mV EW: 0.316 UI	
PCIe Gen4 Spec	Minimum			EH: 15.0 mV EW: 0.30 UI	

Figure 10. Comparison of Channel Eye Diagram Results for PCIe Gen4

END-END 25GBASE-KR/100GBASE-KR4 COMPLIANCE AT 25 GBAUD USING COM (what the heck is COM anyway?)

25GBASE-KR/100GBASE-KR4 performance can be validated utilizing the COM tool that was developed by the IEEE 802.3 working group.

GEN5 Ethernet 100Gbase-KR4 and 25Gbase-KR (25 Gbaud) Channel Requirements are based on Channel Operating Margin (COM), which is a highly complex signal-to-noise figure of merit for a channel derived from a measurement of its scattering parameters. COM is related to the ratio of a calculated signal amplitude to a calculated noise amplitude as defined by Equation (93A–1) in IEEE802.3-2015.

$$\mathrm{COM} = 20\log_{10}(\mathrm{As}/\mathrm{Ani}) \qquad (93A\text{–}1)$$

The signal amplitude As is defined in 93A.1.6 in IEEE802.3-2015 and the noise amplitude Ani is defined in 93A.1.7 in IEEE802.3-2015. The Figure on the next slide which is from 802.3 depicts the COM reference Model.

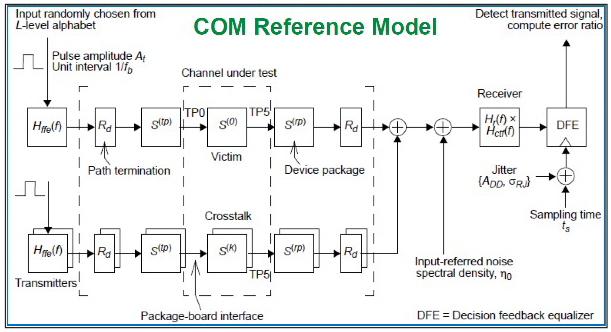


Figure 11. COM Reference Model from IEEE 802.3

The IEEE's open-source COM simulation tool provides turnkey capability for channel assessment, where the user provides the channel characteristics using several touchstone (s-parameter) files for the thru channel and each of the nearby crosstalk aggressors, and the COM simulation tool calculates the Channel Operating Margin (COM) figure of merit.

Unlike lower speed protocols, the channel includes the device packages at both ends. The COM tool optionally adds worst-case device package characteristics to the channel before simulation if an actual device package model is available. See (Figure 12) for the end-end 100GbE channel configuration that we simulated.

Both the short channel and the long channel pass Eye Height and Eye Width requirements for PCIe Gen4 with lots of margin for both the TE spec backplane and the Atrenne backplane, although the Atrenne backplane performs better.

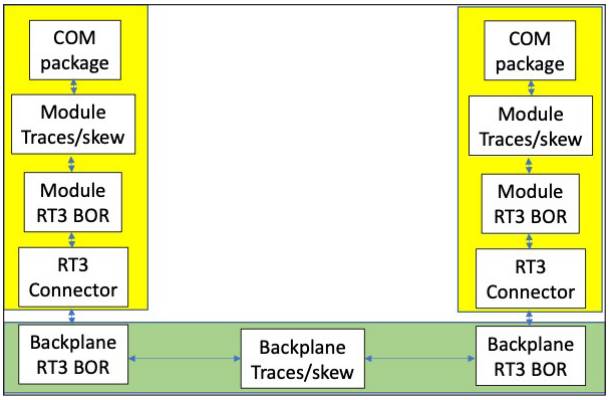


Figure 12. Channel Topology for 25GBASE-KR/100GBASE-KR4 COM Simulations

Per the IEEE 802.3 standard, the COM pass/fail limit is 3 dB minimum. We used COM revision "com_ieee8023_93a" for our analysis.

Here is a Long-Long channel COM plot with Modules at both ends using 6-inch long 5-mil VPX Module traces using Megtron 6 as well as generic VPX Module BOR (break out region) via configurations per TE Connectivity's suggested breakout and via geometries but with longer (6-inch) Module traces. The module channels each include 5 ps worst-case skew and standard COM reference packages.

The backplane in this case is Atrenne's long 14" trace length high-performance backplane including 5 ps worst-case skew.

These results are for even wafer BC victim Rx pair with mismatched Low-High-Low impedances and maximum 15 ps total channel skew. This represents the worst-case configuration using Atrenne's backplane design rules.

As can be seen from the plots, the worst-case (Case 2) COM package passes COM at **3.450 dB** with 3.0 dB limit per IEEE 802.3 for 25GBASE-KR/100 GBASE-KR4. Note that actual device package performance is expected to perform better than the worst-case COM Case 2 package, which would yield even better COM results.

(Figure 13) Here is a Short-Short channel COM plot with Modules at both ends using generic VPX Module BOR (break out region) via configurations per TE Connectivity's suggested breakout and via geometries but with shorter (4-inch) Module traces. The module channels each include 5 ps worst-case skew and standard COM reference packages.

The backplane in this case is Atrenne's minimum trace length high-performance backplane including 5 ps worst-case skew.

These results are for even wafer BC victim Rx pair with mismatched Low-High-Low impedances and maximum 15 ps total channel skew.

We found, as a result of our internal testing and our modeling research, that it is possible to achieve robust Gen-4/5 16/25 Gbaud signaling in OpenVPX systems, but that successful designs require a high degree of care and know-how. It is clear that both the module designs and the backplane designs must be optimized in order to achieve robust Gen-4/5 16/25 Gbaud signaling. The solution rests in commitment to a high level of signal integrity engineering.

As can be seen from the plots, the worst-case COM package passes COM at **5.418 dB** with 3.0 dB limit per IEEE 802.3 for 25GBASE-KR/100 GBASE-KR4.

(Figure 14) Here is a Long-Long channel COM plot with Modules at both ends using generic BOR (break out region) via configurations per TE Connectivity's

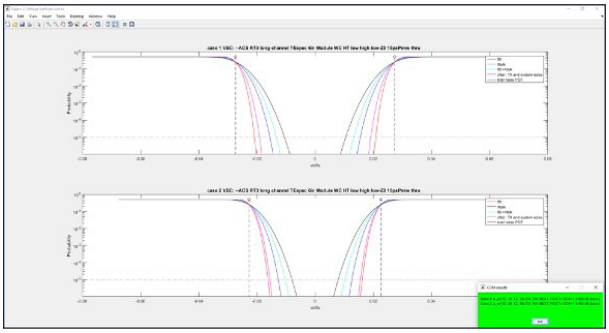


Figure 13. Atrenne Long Channel BC Victim Pair COM Results

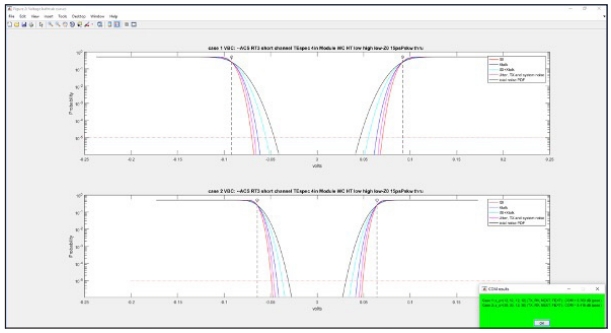


Figure 14. Atrenne Short Channel BC Victim Pair COM Results

suggested breakout and via geometries but with longer (6-inch) Module traces. The module channels each include 5 ps worst-case skew and standard COM reference packages.

The Generic backplane in this case is a backplane using generic BOR (break out region) via configurations per TE Connectivity's suggested breakout and via geometries and the same long 14" trace length as Atrenne's high-performance backplane including 5 ps worst-case skew.

These results are for even wafer BC victim Rx pair with mismatched Low-High-Low impedances and maximum 15 ps skew. This represents the worst-case configuration.

As can be seen from the plots, the worst-case COM package just barely passes COM at 3.032 dB with 3.0 dB limit per IEEE 802.3 for 25GBASE-KR/100 GBASE-KR4.

(Figure 15) is a Short-Short channel COM plot with Modules at both ends using generic BOR (break out region) via configurations per TE Connectivity's suggested breakout and via geometries but with shorter (4-inch) Module traces. The module channels each include 5 ps worst-case skew and standard COM reference packages.

The Generic backplane in this case is a backplane using generic BOR (break out region) via configurations per TE Connectivity's suggested breakout and via geometries and the same minimum trace length as Atrenne's high-performance backplane including 5 ps worst-case skew.

These results are for even wafer BC victim Rx pair with mismatched Low-High-Low impedances and maximum 15 ps skew. This represents the worst-case configuration using Atrenne's backplane design rules.

As can be seen from the plots, the worst-case COM package passes COM at 5.116 dB with 3.0 dB limit per IEEE 802.3 for 25GBASE-KR/100 GBASE-KR4.

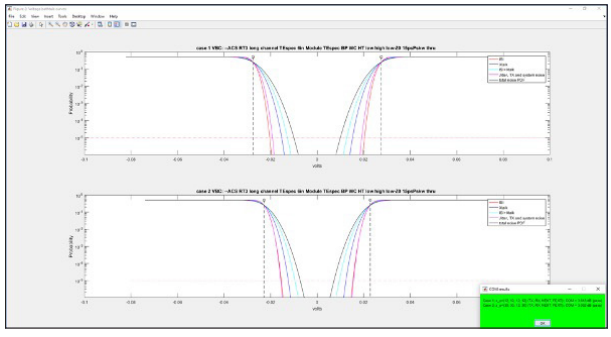


Figure 15. TE-spec Long Channel BC Victim Pair COM Results

Case	Module	Backplane	Conn	COM Case 2 Results	Compare Results
Long	TE spec	Atrenne	RT3	3.450 dB	Atrenne 0.418 dB better
Long	TE spec	TE spec	RT3	3.032 dB	
Short	TE spec	Atrenne	RT3	5.418 dB	Atrenne 0.302 dB better
Short	TE spec	TE spec	RT3	5.116 dB	
PCIe Gen4 Spec			Min	**3.0 dB**	

Figure 17. Comparison of Channel COM Results for 25GBASE-KR/100GBASE-KR4

(Figure 17) The following table compares results with a generic backplane (using BOR model based

on geometries documented in TE Connectivity's RT3 routing guidelines) and Atrenne's high-performance backplane. All cases use generic VPX Modules (using BOR model based on geometries documented in TE Connectivity's RT3 routing guidelines).

The short channel passes COM with lots of margin for both the TE spec backplane and the Atrenne backplane, although the Atrenne backplane performs better.

The significant difference shows up for the long channel, where the Atrenne backplane passes COM with significant margin, outperforming the marginally passing TE spec backplane by 0.418 dB.

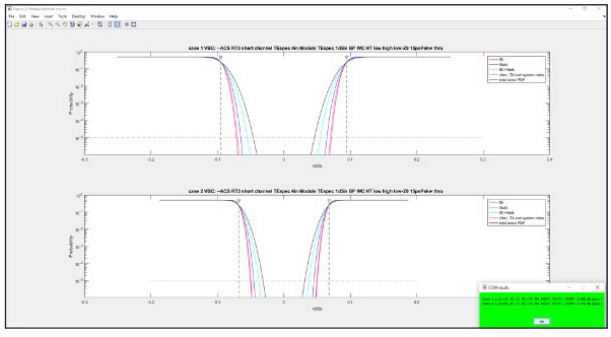


Figure 16. TE-spec Short Channel BC Victim Pair COM Results

We found, as a result of our internal testing and our modeling research, that it is possible to achieve robust Gen-4/5 16/25 Gbaud signaling in OpenVPX systems, but that successful designs require a high degree of care and know-how. It is clear that both the module designs and the backplane designs must be optimized in order to achieve robust Gen-4/5 16/25 Gbaud signaling. The solution rests in commitment to a high level of signal integrity engineering. This makes it imperative that you verify that your suppliers and internal development teams have the necessary tools and know-how required to perform the SI engineering needed to ensure that your next OpenVPX system can perform optimally with Gen-4/5 signaling at 16/25 Gbaud, worst-case with manufacturing variation and across the deployed product temperature range and fiber weave skew variation. Anyone who is not using a high-end industry standard 3D field solver such as HFSS for Gen4/Gen5 designs will have some unpleasant surprises when the rubber hits the road.

For help with your next OpenVPX design please contact Atrenne Computing Solutions. Our simulation-based robust design rules for Gen-4/5 OpenVPX modules and backplanes provide reliable operation at Gen-4/5 signaling rates.

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